ABSTRACT

A multiple agent system providing each of a plurality of agents, e.g., processors, to access a shared synchronous or asynchronous memory. In the case of synchronous memory, the clock signal from a super agent selected from among the plurality of agents provides a memory access clock signal to the other agents accessing the same shared memory. The other agents synchronize their respective address, data and control busses to those of the super agent, and output a representation of the same clock signal to the shared memory. In another aspect of the present invention, the shared memory is partitioned for use from among a plurality of groups of agents, each agent group comprising one or more agents. Any one of the agents may update a configuration register to flexibly reconfigure the amount of shared memory available to the agents as necessary.